



Syfer Technology Limited, Old Stoke Road,
Arminghall, Norwich, Norfolk, NR14 8SQ,
United Kingdom
Tel: +44 (0) 1603 723300.
Tel. (Sales): 01603 723310
Fax: +44 (0) 1603 723301
Email: sales@syfer.co.uk
Web: www.syfer.com

Surface Treated Capacitors To Reduce Surface Arcing

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Introduction

During Voltage Proof/DWV testing of high voltage capacitors arcing can occur across the surface between terminations. The phenomenon of surface arcing is caused by a high voltage gradient between the termination and the internal electrode of opposing polarity.

The high $\delta V/\delta X$ causes ionisation of air molecules resulting in a low resistance path on which the arcing can initiate. This reduces the level of the voltage seen by the part and also leaves a carbon track mark on the surface of the capacitor. Syfer utilise several design variations over standard product in order to reduce the $\delta V/\delta X$ and therefore reduce the susceptibility of our high voltage parts to surface arcing.



The problem of surface arcing occurs most frequently with X7R dielectric material when used with no clean fluxes in high humidity environments at voltage levels of 500V and above.

There are many solutions to this problem; some are more effective than others.

The best solution for protection against surface arcing is to conformally coat the PCB after the population process is complete; this is very effective at preventing arcing but is an extra process which adds expense.

Another solution is to conformally coat the capacitors prior to soldering; this process cannot be undertaken on bulk product because of difficulties in preventing the terminations becoming coated, with detrimental effect to solderability. The process required to overcome this issue is prohibited by cost and time.

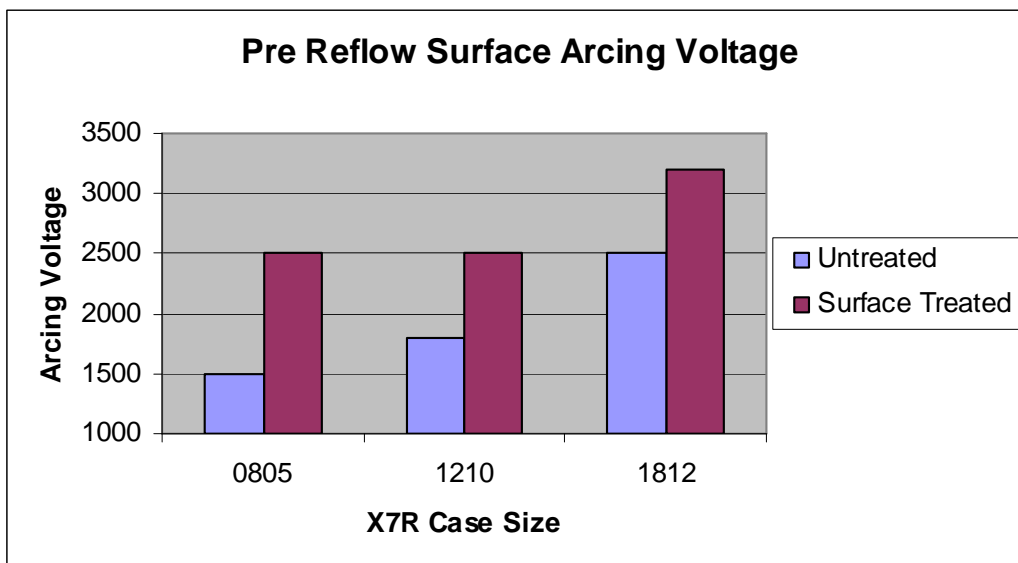
Post soldering cleaning can help prevent arcing; however it is not always the cure and is also another process stage which adds cost.

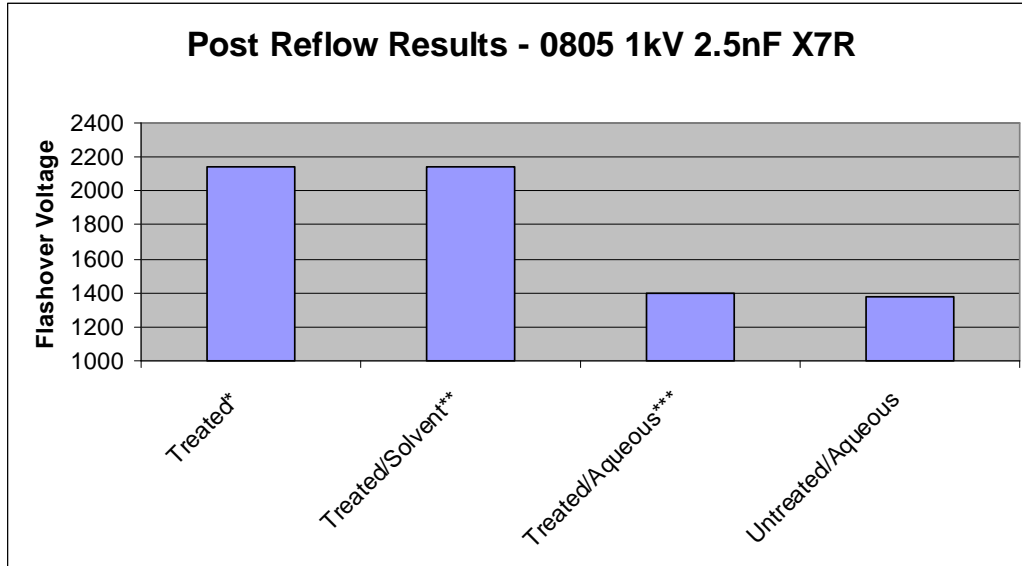


Surface Treatment

In order to further improve the surface arcing resistant capabilities of our high voltage chip capacitors Syfer have developed a surface treatment process which is capable of increasing the Voltage level a capacitor can accommodate before surface arcing occurs. This treatment is applied to the components in a bulk process and achieves the benefit without causing any detrimental effects to the solderability, or any other characteristics of the termination.

Results are summarised below and show a significant improvement in surface arcing performance over several case sizes.





* Voltage limited by internal breakdown

**Solvent Clean used: 3M HFE IPA + Hydrocarbon + Ultrasonic Agitation, Voltage limited by internal breakdown

***Aqueous Clean used: Dr O.K. Wack Vigon US + Ultrasonic Agitation

Testing has shown significantly improved arcing resistance over standard parts when subjected to Voltage Proof/DWV testing post assembly with a reflow process using Indium Corporation of America 60/40 SnPb solder paste with NC-SMQ51SC flux.

Applications

Syfer Surface Treated Capacitors are intended for use in all applications using reflow soldering where post soldering cleaning is not undertaken. The additional surface arcing resistant properties of the parts will be negated by exposure to solder wave and also by aqueous cleaning. The most benefit is likely to be seen at the post assembly voltage proof test stage when the parts are subjected to the dielectric withstand voltage. Testing at Syfer has shown significantly improved surface arcing resistance over standard parts when subjected to Voltage Proof/DWV testing after assembly on boards with a reflow process.



Ordering Information

The surface treated capacitors can be ordered by using a standard Syfer product code with the suffix code PL1.

Example: **1206Y2K00102KXT**PL1****

1206	Case Size
Y	Polymer Termination
2K0	2kV DC Rated
0102	1000pF Capacitance Value
K	10% Capacitance Tolerance
X	X7R Dielectric
T	Taped and Reeled
PL1	Surface Treated to Reduce Surface Arcing

All other specifications and properties are as Syfer standard product.
For further information or technical assistance please contact our Sales Department on +44 1603 723310 or by Email at sales@syfer.co.uk