

Multilayer Ceramic Capacitors are generally divided into classes which are defined by the capacitance temperature characteristics over specified temperature ranges. These are designated by alpha numeric codes. Code definitions are summarised below and are also available in the relevant national and international specifications.

COG/NPO - Ultra Stable Class 1 Ceramic (EIA Class 1)

Spec.	Classification	Temperature range °C	Maximum capacitance change	Syfer dielectric code
CECC	1B/CG	-55 +125	0 ± 30ppm/°C	C
EIA	COG/NPO	-55 +125	0 ± 30ppm/°C	C
MIL	CG (BP)	-55 +125	0 ± 30ppm/°C	C

Capacitors within this class have a dielectric constant range from 10 to 100. They are used in applications which require ultra stable dielectric characteristics with negligible dependence of capacitance and dissipation factor with time, voltage and frequency. They exhibit the following characteristics:-

- a) Time does not significantly affect capacitance and dissipation factor (Tan δ) – no ageing.
- b) Capacitance and dissipation factor are not affected by voltage.
- c) Linear temperature coefficient.

X8R, X7R and X5R - Stable Class II Ceramic (EIA Class II)

Spec.	Classification	Temperature range °C	Maximum capacitance change % over temperature range		Syfer dielectric code
			No DC volt applied	Rated DC Volt	
CECC	2C1	-55 +125	±20	+20 -30	R
	2R1	-55 +125	±15	- -	X
	2X1	-55 +125	±15	+15 -25	B
EIA	X8R	-55 +150	±15	- -	N
	X7R	-55 +125	±15	- -	X
	X5R	-55 +85	±15	- -	P
MIL	BX	-55 +125	±15	+15 -25	B
	BZ	-55 +125	±20	+20 -30	R

Capacitors of this type have a dielectric constant range of 1000-4000, and also have a non-linear temperature characteristic which exhibits a dielectric constant variation of less than ±15% (2R1) from its room temperature value, over the specified temperature range. Generally used for by-passing (decoupling), coupling, filtering, frequency discrimination, DC blocking and voltage transient suppression

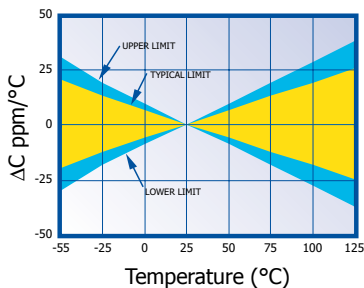
with greater volumetric efficiency than Class I units, whilst maintaining stability within defined limits.

Capacitance and dissipation factor are affected by:-
 Time (Ageing)
 Voltage (AC or DC)
 Frequency

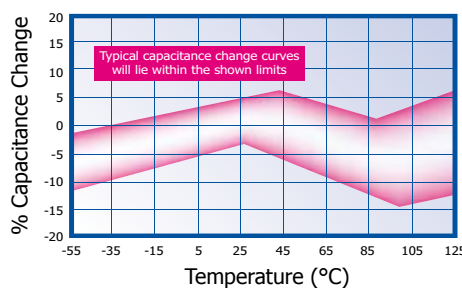
Typical dielectric temperature characteristics

Power ratings

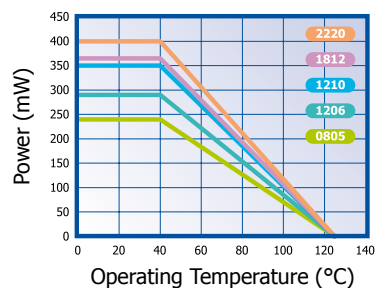
COG/NPO capacitance vs temperature



X7R capacitance vs temperature



COG/NPO and X7R



Technical Summary

	COG/NPO			X5R	X7R			X8R
Dielectric characteristics	Ultra stable			Stable	Stable			Stable
IECQ-CECC	1B/CG	-	-	-	2C1	2R1	2X1	-
EIA	-	COG/NPO	-	X5R	-	X7R	-	X8R
MIL	-	-	CG (BP)	-	BZ	-	BX	-
Rated temperature range	-55°C to +125°C			-55°C to +85°C	-55°C to +125°C			-55°C to +150°C
Maximum capacitance change over temperature range No DC voltage applied	0 ± 30 ppm/°C			± 15%	± 20%	± 15%	± 15%	± 15%
Rated DC voltage applied				-	+20 -30%	-	+15 -25%	-
Syfer dielectric ordering code	C			P	R	X	B	N
Tangent of loss angle (tan δ)	Cr > 50pF ≤ 0.0015 Cr ≤ 50pF = 0.0015 $\left(\frac{15}{Cr} + 0.7\right)$			≤ 0.025	≤ 0.025			≤ 0.025
Insulation resistance (Ri) Time constant (Ri x Cr) (whichever is the least)	100G Ω or 1000s			100G Ω or 1000s	100G Ω or 1000s			100G Ω or 1000s
Capacitance tolerance	Cr < 10pF	± 0.05pF (H) ± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D) ± 1.0pF (F) ± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)		± 5% (J) ± 10% (K) ± 20% (M)	± 5% (J) ± 10% (K) ± 20% (M)			± 5% (J) ± 10% (K) ± 20% (M)
	Cr ≥ 10pF	± 1.0pF (F) ± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)						
Dielectric strength	Voltage applied for 5 seconds. Charging current limited to 50mA maximum.							
≤200V	2.5 times		2.5 times	2.5 times			2.5 times	
>200V to <500V	Rated voltage + 250V		-	Rated voltage + 250V			-	
500V to ≤1000V	1.5 times		-	-			-	
500V to <1000V	-		-	1.5 times			-	
>1kV to ≤1200V	1.25 times		-	-			-	
>1200V	1.2 times		-	-			-	
≥1000V	-		-	1.2 times			-	
Climatic category (IEC)								
Chip	55/125/56		55/85/56	55/125/56			55/150/56	
Dipped	55/125/21		-	55/125/21			-	
Discoidal	55/125/56		-	55/125/56			-	
Ageing characteristic (Typical)	Zero		<2% per time decade	<2% per time decade			<2% per time decade	

The table above highlights the difference in coding for IECQ-CECC, EIA and MIL standards when defining the temperature coefficient and the voltage coefficient.

Approvals

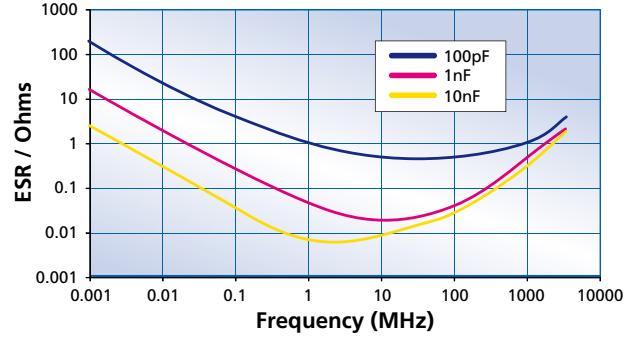
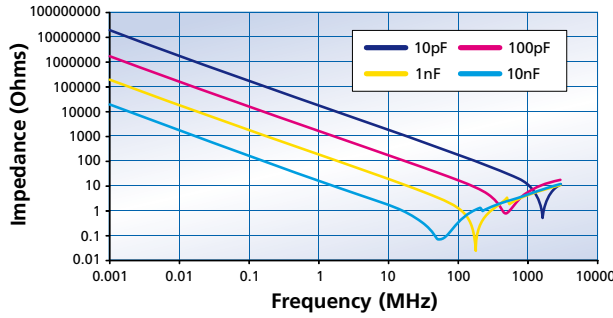
Chip	QC-32100	-	QC-32100	-
Dipped radial	IECQ-CECC 30601-008	-	IECQ-CECC 30701-013	-

Impedance vs Frequency - chips

ESR vs Frequency - chips

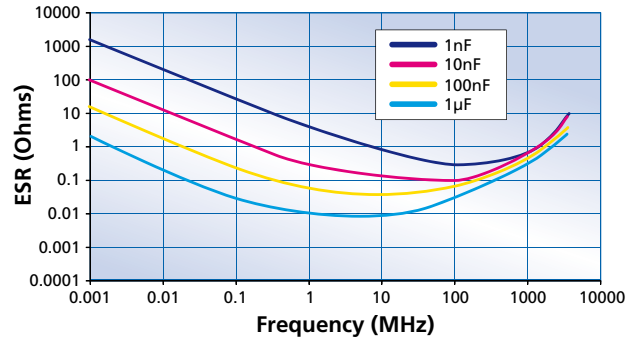
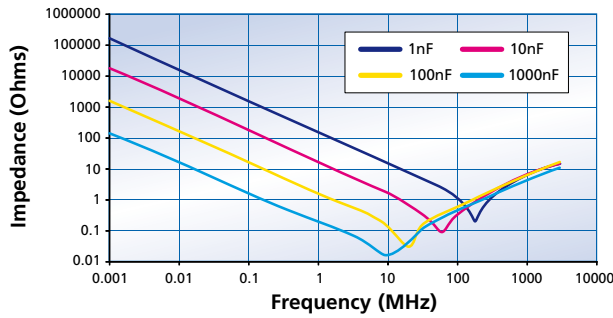
Ultra Stable C0G/NP0 dielectric

Ultra Stable C0G/NP0 dielectric



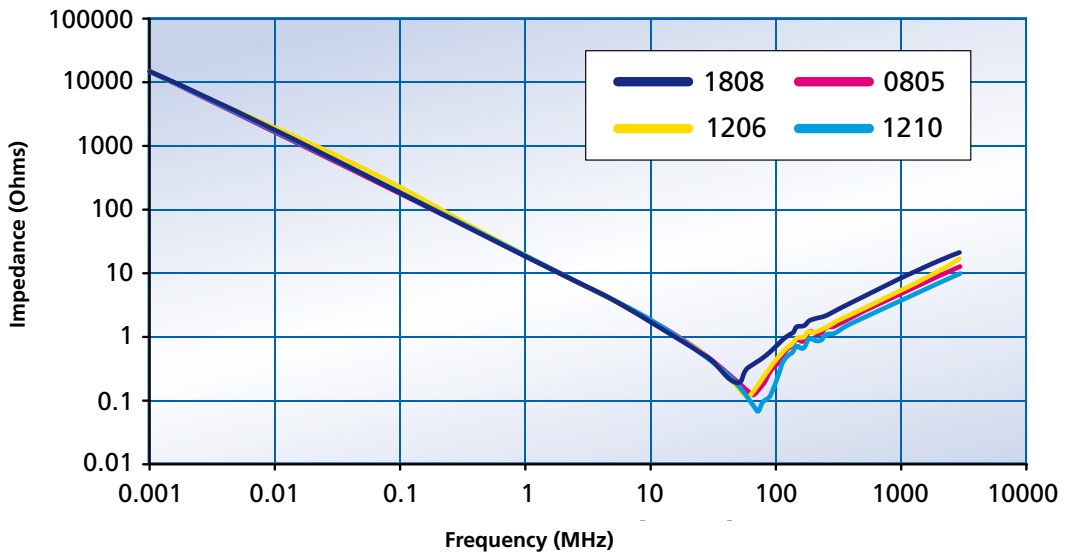
Stable X7R dielectric

Stable X7R dielectric



Impedance vs Frequency - 10nF chips

Stable X7R dielectric



Ageing

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125°C. This domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that in a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

- a) 1% between 1 and 10 hours
- b) An additional 1% between the following 10 and 100 hours
- c) An additional 1% between the following 100 and 1000 hours
- d) An additional 1% between the following 1000 and 10000 hours etc
- e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our Multilayer Ceramic Capacitors are:

Dielectric class	Typical values
Ultra Stable C0G/NP0	Negligible capacitance loss through ageing
Stable X7R	<2 % per decade of time

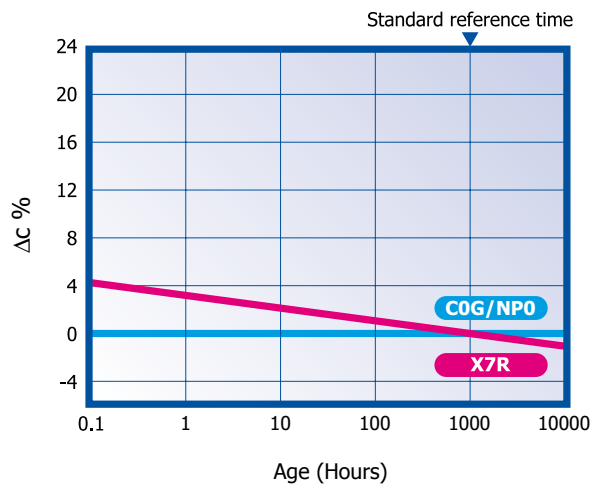
Capacitance measurements

Because of ageing it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs time
(Ageing X7R @ 1% per decade)



Tight tolerance

One of the advantages of Syfer's unique 'wet process' of manufacture is the ability to offer capacitors with exceptionally tight capacitance tolerances.

The accuracy of the printing screens used in the fully automated, computer controlled manufacturing process allows for tolerance as close as +/-1% on C0G/NP0 parts greater than or equal to 10pF. For capacitance values below 10pF, tolerances can be as tight as +/-0.05pF.

