

Notes intended to guide and assist our customers in using multilayer ceramic capacitors in surface mount technology are available from Syfer.

The information concentrates on the handling, mounting, connection, cleaning, test and re-work requirements particular to MLC's for SMD technology, to ensure a suitable match between component capability and user expectation. Some extracts are given below.

**Handling**

Ceramics are dense, hard, brittle and abrasive materials. They are liable to suffer mechanical damage, in the form of chips or cracks, if improperly handled.

Terminations will be abraded onto chip surfaces if loose chips are tumbled in bulk. Metallic tracks will be left on the chip surfaces which might pose a reliability hazard.

Surface mount MLC's should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.

MLC's should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and may leave abraded metal tracks on the product surface. Plastic or plastic coated metal type are readily available and recommended - these should be used with an absolute minimum of applied pressure.

Counting or visual inspection of MLC's is best performed on a clean glass or hard plastic surface.

If MLC's are dropped or subjected to rough handling, they should be visually inspected before use. Electrical inspection may also reveal gross damage via a change in capacitance, an increase in dissipation factor or a decrease either in insulation resistance or electrical strength.

**Transportation**

Where possible, any transportation should be carried out with the product in its unopened original packaging. If already opened, any environmental control agents supplied should be returned to packaging and the packaging re-sealed.

Avoid paper and card as a primary means of handling, packing, transportation and storage of loose chip capacitors. Many grades have a sulphur content which will adversely affect termination solderability.

Loose chips should always be packed with sulphur-free wadding to prevent impact or abrasion damage during transportation.

**Storage**

Incorrect storage of surface mount MLC's can lead to problems for the user.

Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist air, can result in termination oxidation.

Packaging should not be opened until the MLC's are required for use. If opened, the pack should be re-sealed as soon as is practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40 and 60% R.H.

Taped product should be stored out of direct sunlight, which might promote a deterioration in tape or adhesive performance.

Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

**Mechanical considerations for mounted ceramic chip capacitors**

Due to their brittle nature, ceramic chip capacitors are more prone to excesses of mechanical stress than other components used in surface mounting.

One of the most common causes of failure is directly attributable to bending the printed circuit board after solder attachment. The excessive or sudden movement of the flexible circuit board stresses the inflexible ceramic block causing a crack to appear at the weakest point, usually the ceramic/termination interface. The crack may initially be quite small and not penetrate into the inner electrodes; however, subsequent handling and rapid changes in temperature will cause the crack to enlarge.

This mode of failure is often invisible to normal inspection techniques as the resultant cracks usually lie under the capacitor terminations and if left, can lead to catastrophic failure. More importantly, mechanical cracks, unless they are severe will not be detected by normal electrical testing of the completed circuit, failure only occurring at some later stage after moisture ingression.

The degree of mechanical stress generated on the printed circuit board is dependent upon several factors including the board material and thickness, the amount of solder and land pattern. The amount of solder applied is important, as an excessive amount reduces the chip's resistance to cracking.

As to where board flexing occurs sufficiently to produce mechanical stress cracks, it is Syfer's experience that more than 90% are due to board depanelisation, a process where two or more circuit boards are separated after soldering is complete. Other manufacturing stages that should be reviewed include:-

- 1) Attaching rigid components such as connectors, relays, display panels, heat sinks etc.
- 2) Fitting conventional leaded components. Special care must be exercised when rigid terminals, as found on large can electrolytic capacitors, are inserted.
- 3) Storage of boards in such a manner which allows warping.
- 4) Automatic test equipment, particularly the type employing "bed of nails" and support pillars.
- 5) Positioning the circuit board in its enclosure especially where this is a "snap-fit".
- 6) FlexiCap™ is available as a termination option. This is designed to reduce the instances of mechanical cracking.

Further information regarding the mechanical stressing of ceramic multilayer chip capacitors is available on request from our sales office.



### Recommended process temperature - time

The various methods of attachment of chips onto substrates invariably involve thermal cycling and the components may be thermally sensitive. This is particularly true of MLC's. Any temperature steps employed must, in broad terms, be kept below 120°C (248°F) and steps of no more than 70°C (158°F) to 80°C (176°F) are preferred when MLC's, size 1812 and above, are used on the substrate. Ideally the pre-heat zone should elevate the substrate from room temperature to solder operations temperature - in practice, constraints are in place as a result of required process throughput, equipment capability and material properties.

The pre-heat temperature rise of the MLC's should be kept to around 2°C (3.6°F) per second and should be reduced below this when larger chip planforms are used. In practice, successful ranges tend to lie in the area 1.5 to 4°C (2.7 to 7.2°F) per second dependent upon substrate and components.

Actual component temperatures may be verified at various points on the board, by the attachment of fine thermocouples with a bead diameter of no more than 0.25mm. This may be effected using a thermally conductive adhesive. The attachment points should be the upper surface of a component termination for Wave soldering (for re-flow methods, attachment should be made to the component footprint). Use of thru' holes for fixing thermocouples should be avoided.

The introduction of a soak, at the end of the pre-heat, is useful, when larger components are used, as this allows temperature uniformity to be established across the substrate. Soldering a 'cool' substrate may induce substrate warpage. The magnitude or direction of the warpage may change on cooling imposing damaging stresses upon the SMD components.

Solder time should be minimised. The maximum permissible solder time that a surface mounted multilayer ceramic capacitor can be subjected to is dependent upon the termination material and the process temperature characteristics.

For chip sizes 1812 and above, cooling to ambient temperature should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints, very important for large chips. Draughts should be avoided. Forced air cooling can induce thermal breakage, and cleaning with cold fluids immediately after a soldering process may result in cracked MLC capacitors.

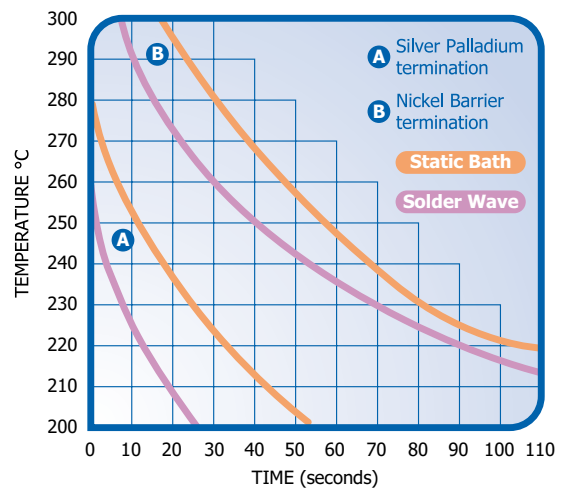
### Solder time (see Fig 1)

Solder melting time should be minimised. The maximum permissible solder time that a surface mounted multilayer ceramic capacitor can be subjected to is dependent upon the termination material and process temperature/time.

Fig 1 shows Comparative Temperature/Time data for silver palladium and nickel barrier terminations to meet the "Solderability Test" as specified for both a static solder bath and a solder wave. These curves should not be exceeded in terms of the maximum exposure time.

### Solder time temperature curves (Fig 1)

Recommended maximum exposure time as a function of temperature.



Successive soldering cycles (including rework) are cumulative in terms of temperature and percentage of time in affecting the capacitor in terms of solderability and resistance to soldering heat.

### Important notes:

1. FlexiCap™ terminations can be processed in the same way as standard nickel barrier types. This is a fully lead free termination.
2. All standard chip capacitors are compatible with lead-free soldering.
3. For RoHS and WEEE status of product, see RoHS compliance section.

### Leaching

Leaching is the term for the dissolution of silver into the solder during the soldering operation. This weakens the terminations leading to an increase in equivalent series resistance (ESR),  $\tan \delta$  and open circuit faults as well as the possibility of the chip becoming detached from the substrate.

To prevent leaching, the following should be observed:-

1. Prework should be kept to a minimum.
2. An adequate preheat period is essential.
3. Solder temperature should be held at the lower end of the normal range.
4. Dwell time should be kept to a minimum.
5. Use ceramic chip capacitors with an "anti-leaching layer". We incorporate a "barrier layer" of nickel in the end terminations to prevent leaching.

### Multilayer ceramic chip - with nickel barrier termination

