

Detailed application notes intended to guide and assist our customers in using multilayer ceramic capacitors in surface mount technology are available on the Syfer website www.syfer.com

The information concentrates on the handling, mounting, connection, cleaning, test and re-work requirements particular to MLC's for SMD technology, to ensure a suitable match between component capability and user expectation. Some extracts are given below.

Handling

Ceramics are dense, hard, brittle and abrasive materials. They are liable to suffer mechanical damage, in the form of chips or cracks, if improperly handled.

Terminations may be abraded onto chip surfaces if loose chips are tumbled in bulk. Metallic tracks may be left on the chip surfaces which might pose a reliability hazard.

Components should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.

Chip capacitors should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and may leave abraded metal tracks on the product surface. Plastic or plastic coated metal types are readily available and recommended - these should be used with an absolute minimum of applied pressure.

Counting or visual inspection of chip capacitors is best performed on a clean glass or hard plastic surface.

If chips are dropped or subjected to rough handling, they should be visually inspected before use. Electrical inspection may also reveal gross damage via a change in capacitance, an increase in dissipation factor or a decrease either in insulation resistance or electrical strength.

Transportation

Where possible, any transportation should be carried out with the product in its unopened original packaging. If already opened, any environmental control agents supplied should be returned to packaging and the packaging re-sealed.

Avoid paper and card as a primary means of handling, packing, transportation and storage of loose components. Many grades have a sulphur content which will adversely affect termination solderability.

Loose chips should always be packed with sulphur-free wadding to prevent impact or abrasion damage during transportation.

Storage

Incorrect storage of components can lead to problems for the user. Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist or polluted air, can result in termination oxidation.

Packaging should not be opened until the MLC's are required for use. If opened, the pack should be re-sealed as soon as is practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40 and 60% R.H.

Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesive performance.

Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

Mechanical considerations for mounted ceramic chip capacitors

Due to their brittle nature, ceramic chip capacitors are more prone to excesses of mechanical stress than other components used in surface mounting.

One of the most common causes of failure is directly attributable to bending the printed circuit board after solder attachment. The excessive or sudden movement of the flexible circuit board stresses the inflexible ceramic block causing a crack to appear at the weakest point, usually the ceramic/termination interface. The crack may initially be quite small and not penetrate into the inner electrodes; however, subsequent handling and rapid changes in temperature may cause the crack to enlarge.

This mode of failure is often invisible to normal inspection techniques as the resultant cracks usually lie under the capacitor terminations but if left, can lead to catastrophic failure. More importantly, mechanical cracks, unless they are severe may not be detected by normal electrical testing of the completed circuit, failure only occurring at some later stage after moisture ingression.

The degree of mechanical stress generated on the printed circuit board is dependent upon several factors including the board material and thickness; the amount of solder and land pattern. The amount of solder applied is important, as an excessive amount reduces the chip's resistance to cracking.

It is Syfer's experience that more than 90% are due to board depanelisation, a process where two or more circuit boards are separated after soldering is complete. Other manufacturing stages that should be reviewed include:

- 1) Attaching rigid components such as connectors, relays, display panels, heat sinks etc.
- 2) Fitting conventional leaded components. Special care must be exercised when rigid terminals, as found on large can electrolytic capacitors, are inserted.
- 3) Storage of boards in such a manner which allows warping.
- 4) Automatic test equipment, particularly the type employing "bed of nails" and support pillars.
- 5) Positioning the circuit board in its enclosure especially where this is a "snap-fit".

Syfer were the first MLCC manufacturer to launch a flexible termination to significantly reduce the instances of mechanical cracking. Flexicap™ termination introduces a certain amount of give into the termination layer absorbing damaging stress. Unlike similar systems, Flexicap™ does not tear under tension, but absorbs the stress, so maintaining the characteristics of the MLCC.

SM Pad Design

Syfer conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should also be considered.

3-Terminal components are not specifically covered by IPC-7351, but recommended pad dimensions are included in the Syfer catalogue / website for these components.



Soldering information

Syfer MLCC's are compatible with all recognised soldering/ mounting methods for chip capacitors. A detailed application note is available on-line at www.syfer.com

Reflow soldering surface mount chip capacitors

Syfer recommend reflow soldering as the preferred method for mounting MLCC's. Syfer MLCC's can be reflow soldered using a reflow profile generally as defined in IPC / JEDEC J-STD-020. Sn/Ni plated termination chip capacitors are compatible with both conventional and lead free soldering, with peak temperatures of 260°C to 270°C acceptable.

The heating ramp rate should be such that components see a temperature rise of 1.5°C to 4°C per seconds to maintain temperature uniformity through the MLCC.

The time for which the solder is molten should be maintained at a minimum, so as to prevent solder leaching. Extended times above 230°C can cause problems with oxidisation of Sn plating. Use of inert atmosphere can help if this problem is encountered. PdAg terminations can be particularly susceptible to leaching with lead free, tin rich solders and trials are recommended for this combination.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

Wave soldering Chip and Radial Leaded capacitors

Wave soldering is generally acceptable, but the thermal stresses caused by the wave have been shown to lead to potential problems with larger or thicker chips. Particular care should be taken when soldering SM chips larger than size 1210 and with a thickness greater than 1.0mm for this reason.

Maximum permissible wave temperature is 270°C for SM chips and 260°C for Radial Leaded capacitors.

The total immersion time in the solder should be kept to a minimum. It is strongly recommended that Sn/Ni plated terminations are specified for wave soldering applications. PdAg termination is particularly susceptible to leaching when subjected to lead free wave soldering and is not generally recommended for this application.

Total immersion exposure time for Sn/Ni terminations is 30s at a wave temperature of 260°C. Note that for multiple soldering operations, including the rework, the soldering time is cumulative.

The pre-heat ramp should be such that the components see a temperature rise of 1.5°C to 4°C per second as for reflow soldering. This is to maintain temperature uniformity through the MLCC and prevent the formation of thermal gradients within the ceramic. The preheat temperature should be within 120°C maximum (100°C preferred) of the maximum solder temperature to minimise thermal shock.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

Rework of Chip capacitors

Syfer recommend hot air/ gas as the preferred method for applying heat for rework. Apply even heat surrounding the component to minimise internal thermal gradients. Soldering irons or other techniques that apply direct heat to the chip or surrounding area, should not be used as these can result in micro cracks being generated.

Minimise the rework heat duration and allow components to cool naturally after soldering.

Hand soldering Radial Leaded capacitors

Radial capacitors can be hand soldered into boards using soldering irons, provided care is taken not to touch the body of the capacitor with the iron tip. Soldering should be carried out from the opposite side of the board to the radial to minimise the risk of damage to the capacitor body. Where possible, a heat sink should be used between the solder joint and the body, especially if longer dwell times are required.

Use of silver loaded epoxy adhesives

Chip capacitors can be mounted to circuit boards using silver loaded adhesive provided the termination material of the capacitor is selected to be compatible with the silver loaded adhesive. This is normally PdAg. Standard tin finishes are often not recommended for use with silver loaded epoxies as there can be electrical and mechanical issues with the joint integrity due to material mismatch.

Solder leaching

Leaching is the term for the dissolution of silver into the solder causing a failure of the termination system which causes increased ESR, $\tan \delta$ and open circuit faults, including ultimately the possibility of the chip becoming detached. Leaching occurs more readily with higher temperature solders and solders with a high tin content. Pb free solders can be very prone to leaching certain termination systems. To prevent leaching, exercise care when choosing solder alloys and minimize both maximum temperature and dwell time with the solder molten.

Plated terminations with nickel or copper anti leaching barrier layers are available in a range of top coat finishes to prevent leaching occurring. These finishes also include Syfer FlexiCap™ for improved stress resistance post soldering.

Multilayer ceramic chip - with nickel barrier termination

